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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

DIVAKARUNI et al.

Serial No.: Not Yet Assigned — Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith — Examiner: Unknown

For: LOGIC SOI STRUCTURE, PROCESS AND APPLICATION FOR VERTICAL BIPOLAR TRANSISTOR

Assistant Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicants are aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,

Frederick W. Gibb, III
Registration No. 37,629

McGinn & Gibb, P.C.
Intellectual Property Law
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22209
(703) 761-4100
Customer No. 21254